**Amendments to the Claims:**

1. (Currently Amended) A system for testing a plurality of test structures, said system comprising a logic circuit which is configured to receive a triggering signal, said logic circuit connectable to a plurality of rows of test structures, said logic circuit configured to sequentially ~~turn on~~ make high a different single row of test structures, each time the triggering signal changes, while the other rows remain ~~off~~ low, wherein only a single row is ~~active~~ high at any given time during the testing and the remaining rows are ~~inactive~~ low, wherein the system is configured to sequentially test the rows of test structures, from a first row to a last row, a single row at a time each time the triggering signal changes.

2. (Original) A system as recited in claim 1, wherein the logic circuit is connectable to 256 rows of test structures.

3. (Original) A system as recited in claim 1, wherein the system is configured to measure transistors, wherein the test structures comprise transistors.

4. (Original) A system as recited in claim 1, wherein the logic circuit is connectable to 256 rows of transistors.

5. (Original) A system as recited in claim 1, wherein the logic circuit comprises a incrementor which is configured to receive the triggering signal.

6. (Original) A system as recited in claim 5, wherein the logic circuit further comprises a decoder which is connected to the incrementor.

7. (Original) A system as recited in claim 6, wherein the decoder is connectable to the rows of test structures.

8. (Original) A system as recited in claim 5, wherein the logic circuit comprises a incrementor and a decoder, said incrementor being configured to receive the triggering signal and having eight output lines, said eight output lines being connected to eight address inputs of said decoder, said decoder having 256 output lines, said 256 output lines being connectable to 256 rows of test structures.

9. (Currently Amended) A method for testing a plurality of test structures, said method comprising: connecting a plurality of rows of test structures to a logic circuit, providing a triggering signal to the logic circuit, wherein the logic circuit selectively turns on the rows of test structures depending on the triggering signal which is received, wherein the logic circuit sequentially ~~turns on~~ makes high a different single row of test structures, each time the triggering signal changes, while the other rows remain ~~off~~ low, wherein only a single row is ~~active~~ high at any given time during the testing and the remaining rows are ~~inactive~~ low, wherein the system is configured to sequentially test the rows of test structures, from a first row to a last row, a single row at a time each time the triggering signal changes.

10. (Original) A method as recited in claim 9, further comprising connecting the logic circuit to 256 rows of test structures.

11. (Original) A method as recited in claim 9, wherein the step of connecting a plurality of rows of test structures to a logic circuit comprises connecting a plurality of transistors to the logic circuit.

12. (Original) A method as recited in claim 9, wherein the step of connecting a plurality of rows of test structures to a logic circuit comprises connecting 256 rows of transistors to the logic circuit.

13. (Original) A method as recited in claim 9, wherein the step of providing a triggering signal to the logic circuit comprises providing the triggering signal to an incrementor.

14. (Original) A method as recited in claim 13, wherein a decoder is connected to the incrementor and said step of connecting a plurality of rows of test structures to the logic circuit comprises connecting the test structures to the decoder.

15. (Previously Presented) A method as recited in claim 13, wherein the incrementor has eight output lines, said eight output lines are connected to eight address inputs of said

decoder, said decoder has 256 output lines, and said 256 output lines are connectable to 256 rows of test structures.

16. (Previously Presented) A system as recited in claim 1, wherein the logic circuit is resettable wherein none of the test structures are turned on.

17. (Previously Presented) A method as recited in claim 9, wherein the logic circuit is resettable wherein none of the test structures are turned on.